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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/340,172	06/25/1999	DEREK CHI-LAN WON		3571

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/340,172	WON, DEREK CHI-LAN	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/20/02* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-86* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *44-77* is/are allowed.

6)☒ Claim(s) *78-86* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claim 78 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (5,903,750).

2. Yeh taught the invention substantially as claimed including a data processing ("DP") system comprising: means and method for storing the history of previous executions of instruction that include predicate predictions (e.g., see col. 3, line 66-col. 4, line 16 and col. 6, lines 55-65, and fig.2a). Yeh also taught using the predicate prediction to predict the target address and generate the instruction pointer (e.g., see fig. 3a). This clearly helps the Yeh system optimize the scheduling of instructions for run-time execution namely using the instructions in the target path or the instructions in the fall through path.

3. Yeh did not expressly detail (claim 78) that the instruction comprised predicate calculation instructions. However, the instructions comprised predicate predictions that comprised information for determining whether a branch instruction was taken or not. Also, Yeh taught using particular algorithms for determining the branch outcome using history data. Therefore it would have been obvious to one of ordinary skill that a calculation of whether the branch was to be taken was made using the predicate. Consequently, it would have been obvious to one of ordinary skill that the Yeh system comprised predicate calculation instructions.

4. Claim 79 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar (6,247,094).

5. Kumar taught the invention substantially as claimed including a data processing ("DP") system comprising: data cache (60)(e.g., see fig.3) data hit/miss table (70)(e.g., see figs. 4,5 and col. 6, line 21-col. 7, line 29).

6. Kumar did not expressly detail (claim 79) that run-time behavior about hit/misses can be recorded to help optimize subsequent instruction scheduling. Kumar however taught the use of the hit/miss table means for prediction of hits to the cache that is updated when an incorrect prediction occurred (e.g., see col. 7, lines 30-61). Therefore it would have been obvious to one of ordinary skill in the DP art that the Kumar system recorded hits/misses in a table means that helped optimize subsequent instruction scheduling especially of memory access instructions (e.g., see col. 8, lines 35-col. 9, line 20).

7. Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moshovos (5,781,752).

8. Moshovos taught the invention substantially as claimed including a data processing ("DP") system comprising: conflict history table means and method for storing load instructions and predictor whether the load instruction should be executed or delay due to dependencies or conflicts (e.g., see col. 3, line 51-col. 4, line 30). Mohoshvos did not specifically detail (claim 80) that the run-time behavior was optimized. However since the Moshovos system provided improved prediction as to when to execute load instructions for preventing dependency conflicts it would have

been obvious to one of ordinary skill that the Moshovos system optimized run-time behavior.

9. Claim 81 is rejected under 35 U.S.C. 103(a) as being unpatentable over Faber (6,105,124)(cited in the last office action) in view of Glew (5,948,097).

10. Faber taught the invention substantially as claimed including a data processing ("DP") system comprising: means and method for mapping an original instruction set to a transformed instruction set (e.g., see col. 3, lines 38-61). Faber did not expressly detail (claim 81) using physical registers to hold results. Glew however taught (e.g., see col. 10, lines 22-50) a table storing mapping of registers and physical registers holding speculative results of execution until they are commited to the logical registers in the register file. Glew also taught performing a call instruction at the end of a procedure and the call instruction performing saving operations in a Pentium processor (e.g., see col. 2, lines 25-45).

11. Faber taught the system was related to the x86 architecture and the processing of instructions in that type system (e.g., see col. 1, line 20-col. 2, line 11): Both Faber and Glew were directed toward the problems of optimizing x86 instructions and processing of instructions in an x86 architecture therefore it would have been obvious to one of ordinary skill to combine the teachings of Faber and Glew (e.g., see col. 2, lines 25-45 of Glew) .

12. Claim 82 is rejected under 35 U.S.C. 103(a) as being unpatentable over Faber (6,105,124)(cited in the last office action) in view of Shiell (5,911,057).

13. Faber taught the invention substantially as claimed including a data processing ("DP") system comprising: means and method for assigning an identifier for the basic block of instructions in memory and marking the transformed instruction set architecture instructions with the corresponding identifier and comparing the identifiers for the basic block and the transformed instructions (e.g., see col. 4, lines 47-60).

14. Faber did not expressly detail (claim 82) use of instruction sequence numbers and commiting instructions in the order of the instruction sequence numbers. Shiell however taught the assigning of instruction sequence numbers (e.g., see col. 6, lines 28-43) and using the instruction sequence numbers for determining if instructions had dependency conflict and determining the order that instructions could be committed for execution and for in-order instruction completion (e.g., see col. 8, lines 44-59).

15. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Faber and Sheill. Faber was directed toward the problems of implementing dynamically translated basic blocks of instructions including where the first instruction set is the x86 instruction set (e.g., see col. 1, lines 20-37). Shiell was direct toward the problems of executing instructions of the x86 instruction set (e.g., see col. 2, lines 48-59) and improving efficiency at handling dependencies (e.g., see col. 3, lines 1-20). Therefore the Faber system clearly taught a system that had to handle dependencies for executing the instructions of either the x86 or other instruction set and it would have been obvious to one of ordinary skill that the combination of the Shiell teachings of the use of sequence numbers to handle dependencies would have improved the processing of the instructions in the Faber system.

16. Claim 83 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moshovos (5,781,752).

17. Moshovos taught the invention substantially as claimed including a data processing ("DP") system comprising: creating and updating of an array that stored potential instruction dependency and instruction prediction data and a synchronization array that stored load/store instruction dependency information for code (e.g., see col. 11, lines 8-62). Also Moshovos taught that the arrays were accessed in the processing of instructions (e.g., see col. 11, lines 8-62).

18. Moshovos did not expressly detail (claim 83) that the access to the tables was for code scheduling. However, the arrays provided information that indicated the dependencies for instructions and this would have been used to determine if one instruction was to be executed or delayed. Therefore it would have been obvious to one of ordinary skill in the DP art that the Moshovos system used the information stored in the arrays for code scheduling.

19. Claim 84 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bharadwaj (5,787,287).

20. Bharadwaj taught the invention substantially as claimed including a data processing ("DP") system comprising: means and method for executing instructions means and method for noting dependencies between instruction by using instruction vectors (e.g., see col. 3, lines 23-67, and col. 4, line 37-col. 5, line 67).

21. Bharadwaj did not expressly detail (claim 84) that the instructions were from an instruction set architecture. However the processing means for Bharadwaj was taught as related to the improving performance in superscalar microprocessors (e.g. see col. 1, lines 13-25). Therefore it would have been obvious to one of ordinary skill that the Bharadwaj instructions were from an instruction set architecture.

22. Claim 85 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bharadwaj (5,787,287).

23. Bharadwaj taught the invention substantially as claimed including a data processing ("DP") system comprising: means and method for executing instructions means and method for noting dependencies between instruction by using instruction vectors (e.g., see col. 3, lines 23-67, and col. 4, line 37-col. 5, line 67). The claims particularize pointers instead of vectors. However, the vectors of Bharadwaj provide the same function of pointing to instructions or data therefore it would have been obvious to one of ordinary skill in the art that the Bharadwaj system comprised instruction pointers for noting dependencies.

24. Bharadwaj did not expressly detail (claim 85) that the instructions were from an instruction set architecture. However the processing means for Bharadwaj was taught as related to the improving performance in superscalar microprocessors (e.g. see col. 1, lines 13-25). Therefore it would have been obvious to one of ordinary skill that the Bharadwaj instructions were from an instruction set architecture.

25. Claim 86 is rejected under 35 U.S.C. 103(a) as being unpatentable over Faber (6,105,124)(cited in the last office action).

26. Faber taught the invention substantially as claimed including a data processing ("DP") system comprising:

Means and method for using a translator stored in memory for code blocks from an original instruction set into a transformed instruction set architecture (e.g., see col. 1,lines 28-37);

Means and method for storing transformed code blocks into a memory (e.g., see fig.1 and col. 2, lines 29-41) or alternatively storing translated blocks in cache (e.g., see col. 4, lines 39-43); and

Means and method for software to translate the code blocks from a first instruction set to a transformed instruction set (e.g., see col. 3, lines 12-27).

27. Faber did not expressly detail (claim 86) that the storing of the transformed code blocks was for possible future execution. Faber however taught fetching, and issuing the translated blocks to an execution unit of the processor and executed (e.g., see col. 4 lines 53-61), and that the probability of taking a block's branch instruction was determined during processing of the block (e.g., see col. 4, lines 53-67). Therefore it would have been obvious to one of ordinary skill in the DP art that in the Faber system the transformed code blocks were stored for possible future execution.

Allowable Subject Matter

28. Claims 44-77 are allowed.

29. Applicant's arguments with respect to claims 78-86 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-3900.

EC
June 10, 2002

ERIC COLEMAN
PRIMARY EXAMINER